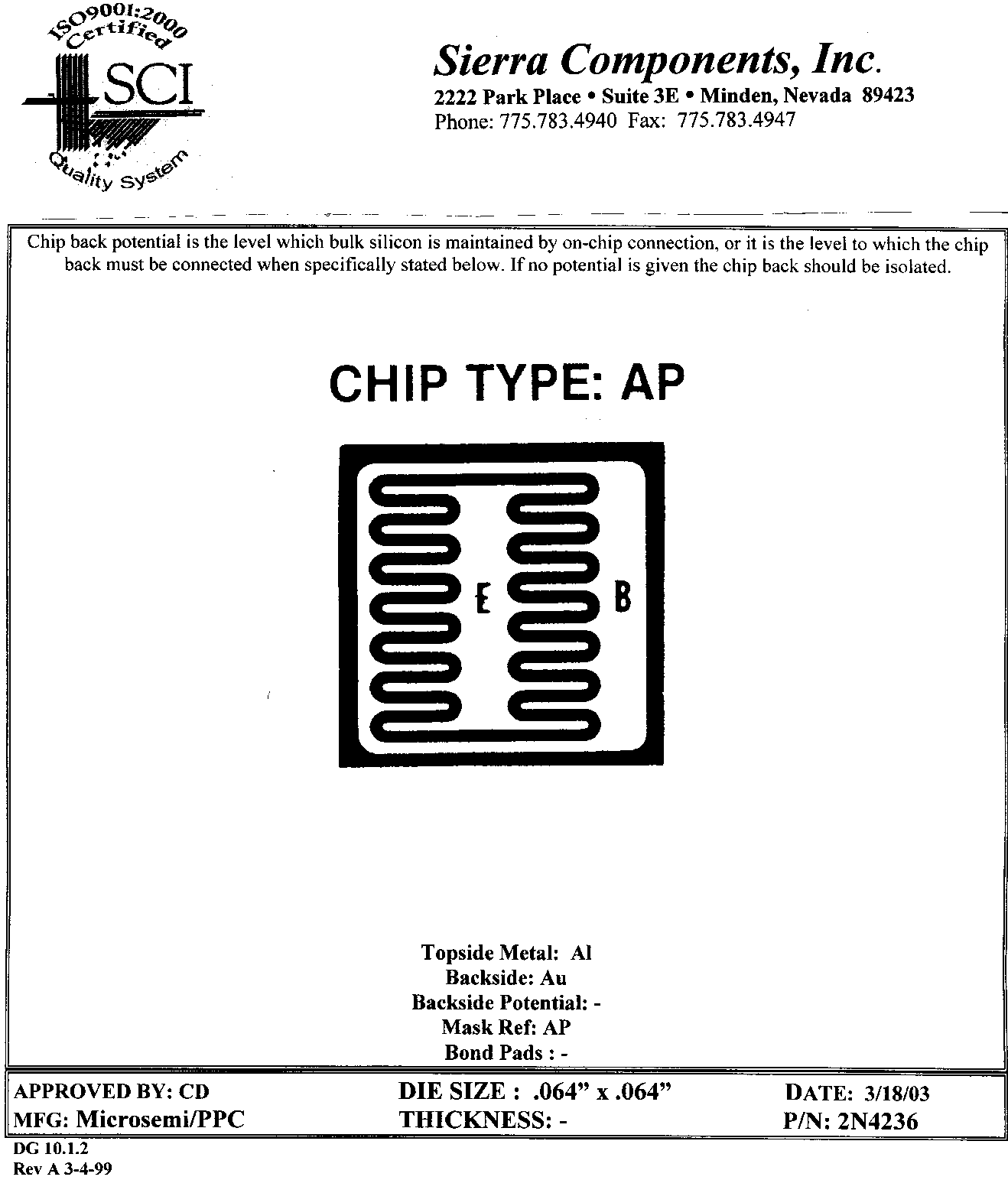
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.064”**

**.064”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004 X .007”**

**Backside Potential: COLLECTOR**

**Mask Ref: AP**

**APPROVED BY: DK DIE SIZE .064” X .064” DATE: 11/17/21**

**MFG: PPC-MICROSEMI THICKNESS .010” P/N: MJEC350**

**DG 10.1.2**

#### Rev B, 7/1